

Customer No.: 31561
Application No.: 10/710,818
Docket No.: 14217-US-PA-X

REMARKS

Present Status of the Application

Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the AAPA of this application in combination with Shokouhi et al. (US patent 6,249,458).

Applicant has amended claim 1 to more clearly define the present invention. After entry of the foregoing amendments, claims 1-10 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Rejections

Applicant respectfully traverses the rejection of claims 1-10 under 103(a) as being unpatentable over AAPA in view of Shokouhi et al. (US patent 6,249,458) because a prima facie case of obviousness has not been established by the Office Action.

To establish a prima facie case of obviousness under 35 U.S.C. 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element in the claims. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must "be found in the prior art, and not be based on applicant's disclosure." See M.P.E.P. 2143, 8th ed., February 2003.

The present invention is in general related an electrostatic discharge (ESD) protection device as claim 1 recites:

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Claim 1. An electrostatic discharge (ESD) protection device, comprising:
an ESD protection circuit, comprising:
at least a diode connected in series between a first voltage and a pad; and
at least an ESD component connected in series between a second voltage and a pad, wherein
each of the at least an ESD component is composed of a deep N-well region formed in a P-type substrate, a triple P-well formed in the deep N-well region, and a highly doped N-type (N+) region and a highly doped P-type (P+) region formed in the triple P-well region, wherein the N+ region of the ESD component is connected to the pad, and the P+ region of the ESD component is connected to the second voltage.

The office action stated applicants have a different reason or advantage resulting from doing what the relied prior art suggested doing is not indicative or demonstrative of unobviousness. Also, the prior art motivation or advantage may be different from that of applicants while still supporting a conclusion of obviousness. However, applicant respectfully disagrees. As a matter of fact, applicant respectfully submits not only prior art references combined do not teach or suggest each and every element in the claims, but also there is not suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to combine the references in a manner resulting in the claimed invention.

Please see col. 7, line 58- col. 8, line 4, Shokouhi teaches FIG. 7 is a cross-sectional side view showing an embodiment of *triple P-well resistors 600*, which is utilized in both first switch 510-B and second switch 530-B (see FIG. 6). Triple P-well resistor 600 is formed in a *P-type substrate (or outer P-well) 710 that is coupled to ground* through a P+ diffused region 711. In P-type substrate 710 is formed a *deep N-well region 720 that is coupled to VCC* through an N+ diffused region 721. Finally, a P-well region 730 is formed in deep N-well region 720, and

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includes a first P+ diffused region 731 forming a first terminal T1, and a second P+ diffused region 733 forming a second terminal T2. As indicated by the dashed resistor symbol, P-well region 730 effectively acts as a resistor extending between first terminal T1 and second terminal T2. Shokouhi also teaches (col. 8, lines 5-16) triple P-well resistor 600 avoids the leakage problems associated with prior art resistor structures because deep N-well 720 is biased to VCC and P-substrate 710 grounded, thereby generating an effective diode 715 at the junction between P-substrate 710 and deep N-well region 720, and an effective diode 735 at the junction between deep N-well region 720 and P-well region 730. Effective diodes 715 and 35 serve to reverse bias the P-well-to-deep N-well junction by approximately 11 to 12 V (assuming VCC is 3.3 V, and the low doped junction breakdown voltage is more than 12 V). Accordingly, negative currents are passed through triple P-well resistor 600 with minimal leakage.

First, the citation discloses two P+ diffused regions 731, 733 are formed in the P-well 730, and the device shown in Fig. 7 is a resistor. In claim 1 of the present application, there are one highly doped N-type (N+) region and one highly doped P-type (P+) region formed in the triple P-well region, and the device including a deep N-well region formed in a P-type substrate, a triple P-well formed in the deep N-well region, and a highly doped N-type (N+) region and a highly doped P-type (P+) region formed in the triple P-well region is an ESD component. The two devices are different in structure and function.

Moreover, the citation teaches the P+ diffused regions 731, 733 are respectively as a first terminal T1 and a second terminal T2, but the P+ diffused regions 731, 733 are not connected to any voltage. In the citation, the deep N-well 720 is biased to VCC and the P-substrate 710 is

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grounded such that an effective diode 715 at the junction between P-substrate 710 and deep N-well region 720, and an effective diode 735 at the junction between deep N-well region 720 and P-well region 730 are generated so as to avoid the leakage problems associated with prior art resistor structures.

In claim 1 of the present application, the N+ region of the ESD component is connected to the pad, and the P+ region of the ESD component is connected to the second voltage. Therefore, the ESD component can be provided for the ESD clamp circuit of the ESD protection circuit, the parasitic capacitance of the ESD clamp circuit is much less than that of the conventional diode string. In addition, since the ESD component does not constructed by the substrate of the ESD clamp circuit of the ESD protection circuit, the problem of the substrate noise may be reduced.

For at least the foregoing reasons, Applicant respectfully submits that the prior references fail to teach or suggest each of the at least an ESD component is composed of a deep N-well region formed in a P-type substrate, a triple P-well formed in the deep N-well region, and *a highly doped N-type (N+) region and a highly doped P-type (P+) region* formed in the triple P-well region, and the *N+ region of the ESD component is connected to the pad, and the P+ region of the ESD component is connected to the second voltage.* The prior art references combined do not teach or suggest each and every element in claim 1.

In addition, the device of Fig. 7 disclosed by Shokouhi is a resistor, and the resistor is different from the ESD component of the present invention in structure and function. Hence, there is not suggestion or motivation, either in the references themselves or in the knowledge

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generally available to one of ordinary skilled in the art, to combine the references in a manner resulting in the claimed invention. In holding an invention obvious in view of a combination of references, there must be some suggestion, motivation, or teaching in the prior art that would have led a person of ordinary skill in the art to select the references and combine them in the way that would produce the claimed invention (*Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1385 (Fed. Cir. 2001)).

Therefore, Applicant respectfully submits a prima facie case of obviousness has not been established by the Office Action. Independent claim 1 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-10 patently define over the prior art as a matter of law.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-10 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted,

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